IN THE CLAIMS:

1. (Currently Amended) A method for manufacturing a semiconductor device, comprising:

forming a polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon gate electrode;

forming a blocking layer over said source/drain regions in a step, said blocking layer comprising a metal silicide;

siliciding said polysilicon gate electrode to form a silicided gate electrode in a different step.

2. (Currently Amended) The method as recited in Claim 1 wherein said ~~forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode~~ step occurs prior to said different step.

3. (Original) The method as recited in Claim 1 wherein said blocking layer is a silicided source/drain contact region.

4. (Original) The method as recited in Claim 1 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

5. (Original) The method as recited in Claim 4 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

6. (Original) The method as recited in Claim 1 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

7. (Original) The method as recited in Claim 1 further including forming a protective layer over said polysilicon gate electrode prior to said forming a blocking layer over said source/drain regions.

8. (Original) The method as recited in Claim 7 wherein said protective layer is a silicon nitride protective layer.

9. (Original) The method as recited in Claim 1 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.

10. (Currently Amended) A method for manufacturing an integrated circuit, comprising:

forming semiconductor devices over a substrate, including;

forming a polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon gate electrode;

forming a blocking layer over said source/drain regions in a step, said blocking layer comprising a metal silicide;

siliciding said polysilicon gate electrode to form a silicided gate electrode in a

different step; and

forming interconnects within dielectric layers located over said substrate for electrically contacting said semiconductor devices.

11. (Currently Amended) The method as recited in Claim 10 wherein said ~~forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode~~ step occurs before said different step.

12. (Original) The method as recited in Claim 10 wherein said blocking layer is a silicided source/drain contact region.

13. (Original) The method as recited in Claim 10 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

14. (Original) The method as recited in Claim 13 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

15. (Original) The method as recited in Claim 10 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

16. (Original) The method as recited in Claim 10 further including forming a protective layer over said polysilicon gate electrode prior to said forming a blocking layer over said source/drain regions.

17. (Original) The method as recited in Claim 16 wherein said protective layer is a

silicon nitride protective layer.

18. (Original) The method as recited in Claim 10 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.